

FIG. 1

	WAYS			
	0	1	2	3
0000000000000001				
0000000000000010				
⋮				
1111111111111111				

201

FIG. 2

INDICES

100T50" 8E2E980

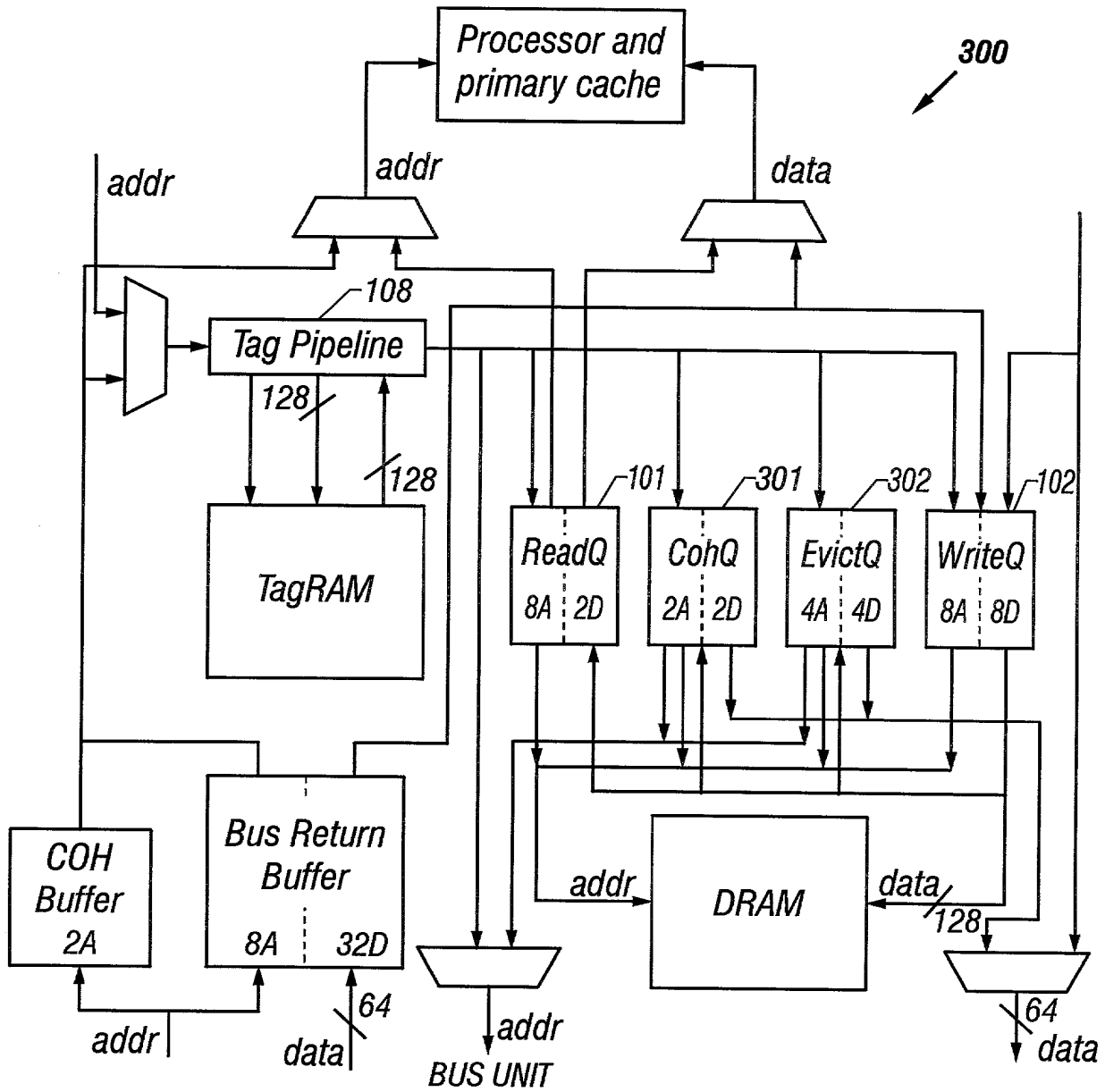


FIG. 3

4/10

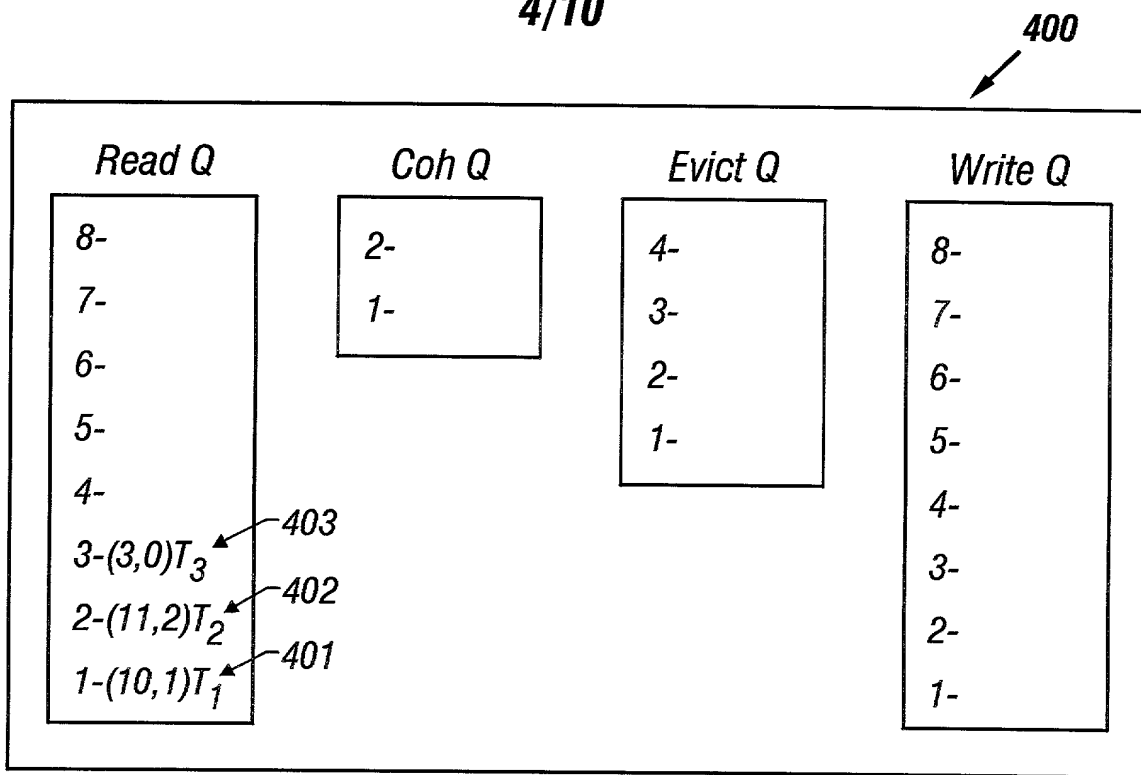


FIG. 4

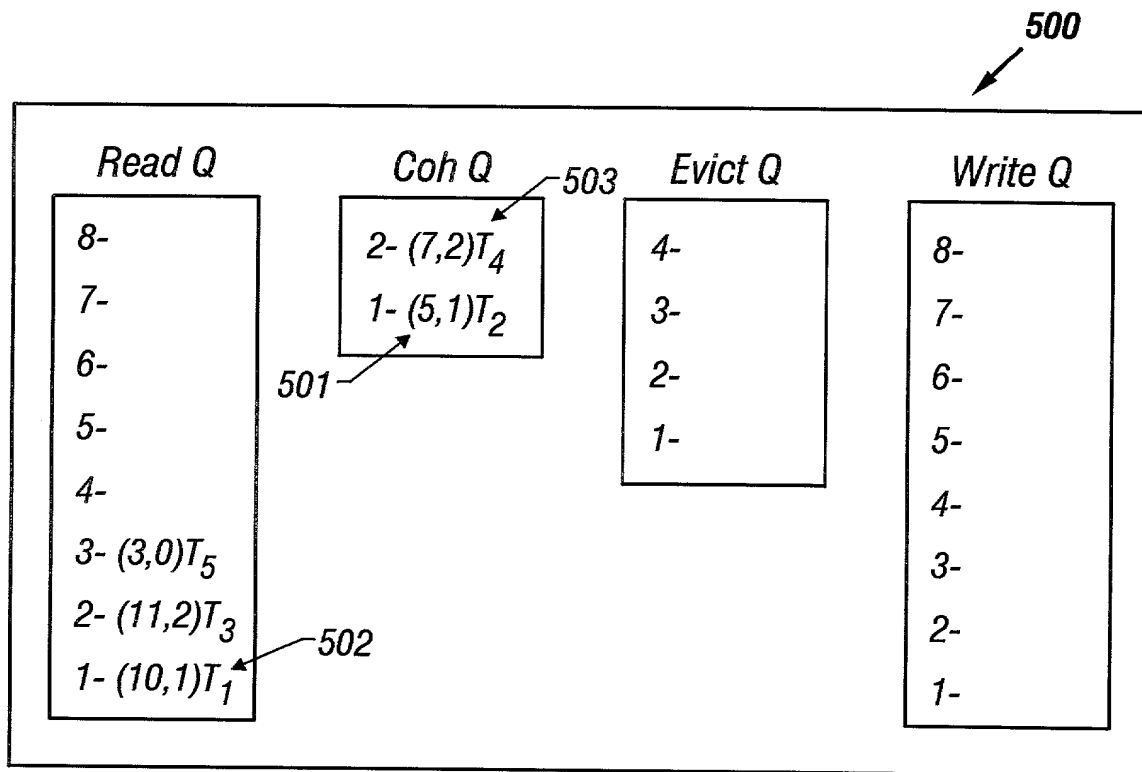


FIG. 5

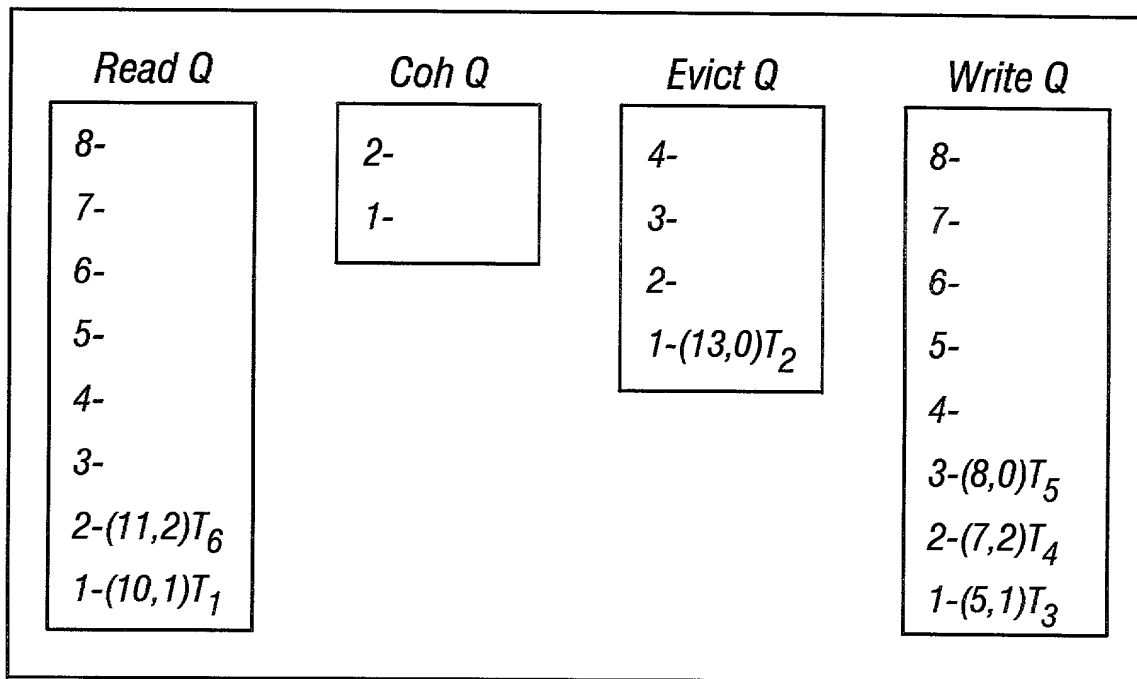


FIG. 6

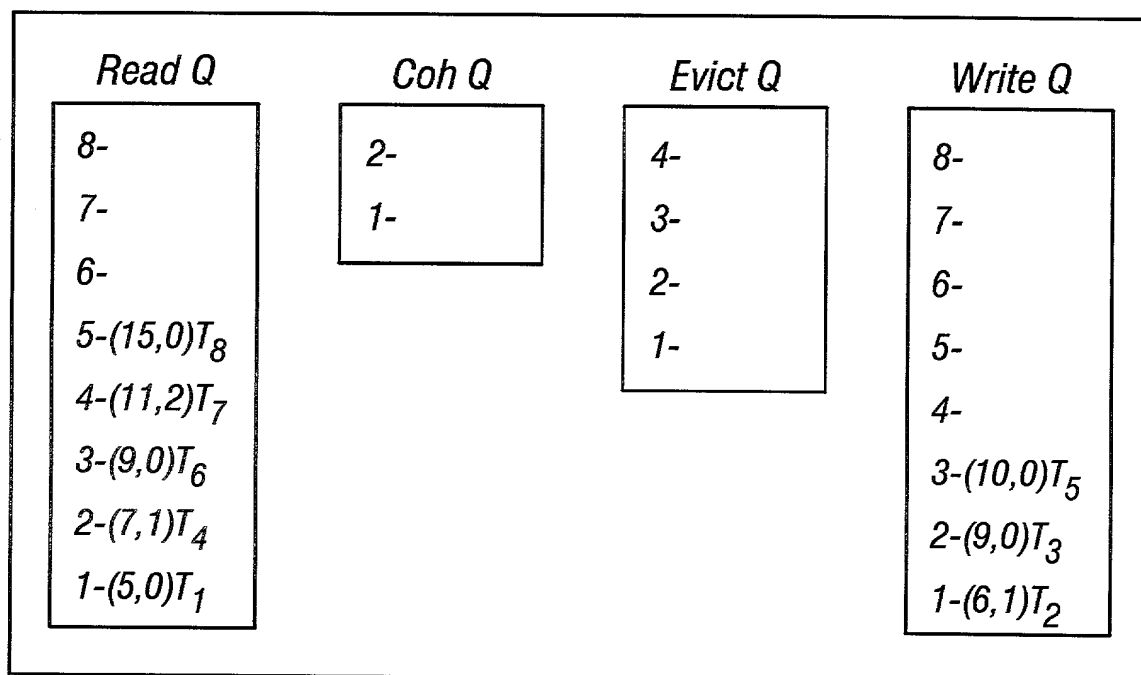


FIG. 7A

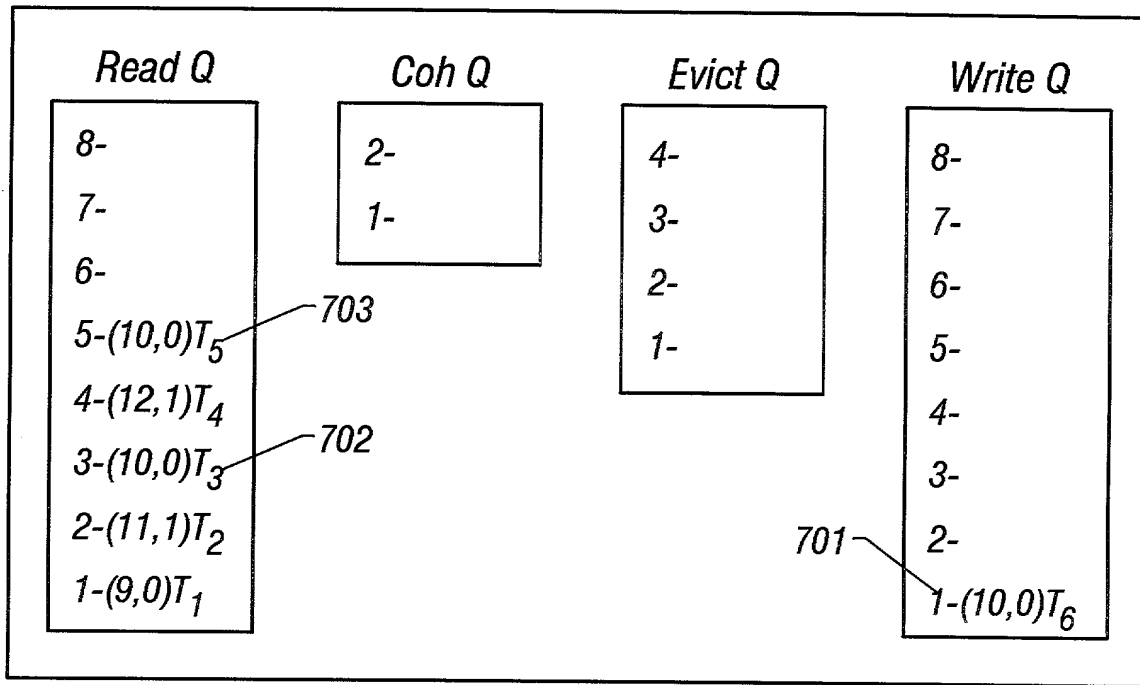


FIG. 7B

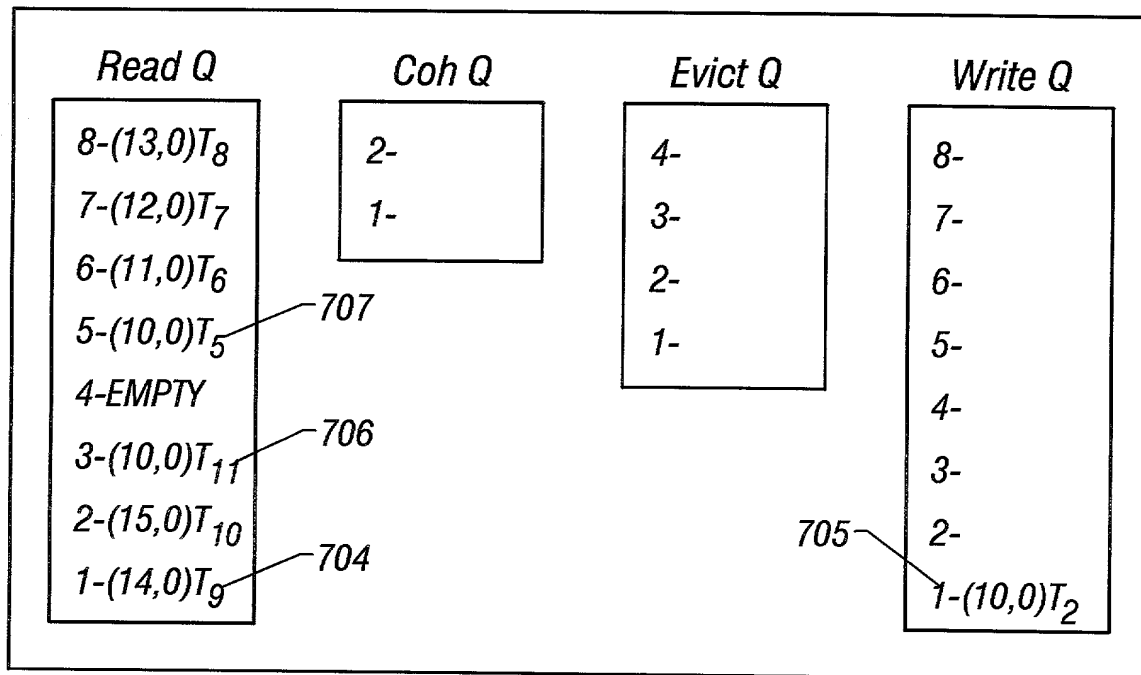


FIG. 7C

**Second (Next)**

Transactions on a single DRAM Address	Read Q	Coh Q	Evict Q	Write Q
Read Q	In order <u>803</u>	DC <u>808</u>	DC <u>807</u>	Dependency ensures read first, write second <u>814</u>
Coh Q	DC <u>812</u>	In order <u>804</u>	DC <u>809</u>	Handled by priority <u>816</u>
Evict Q	DC <u>811</u>	DC <u>810</u>	In order <u>805</u>	Evict first write second dependency <u>818</u>
Write Q	Write first Read second Dependency <u>813</u>	Dependency between Coh and Write Coh waits <u>815</u>	Write first Evict second Dependency <u>817</u>	In order <u>806</u>

**First (Pending)**

FIG. 8

900		901	
	ORIGINAL MATCH BITS	0001	0100
902	COUNTER VALUE = 3		
903	RIGHT SHIFTED BITS	1000	0010
904	CLEAR MASK	0111	1111
	APPLIED MASK	1000	0000
	REVERSE SHIFT	0000	0100

FIG. 9

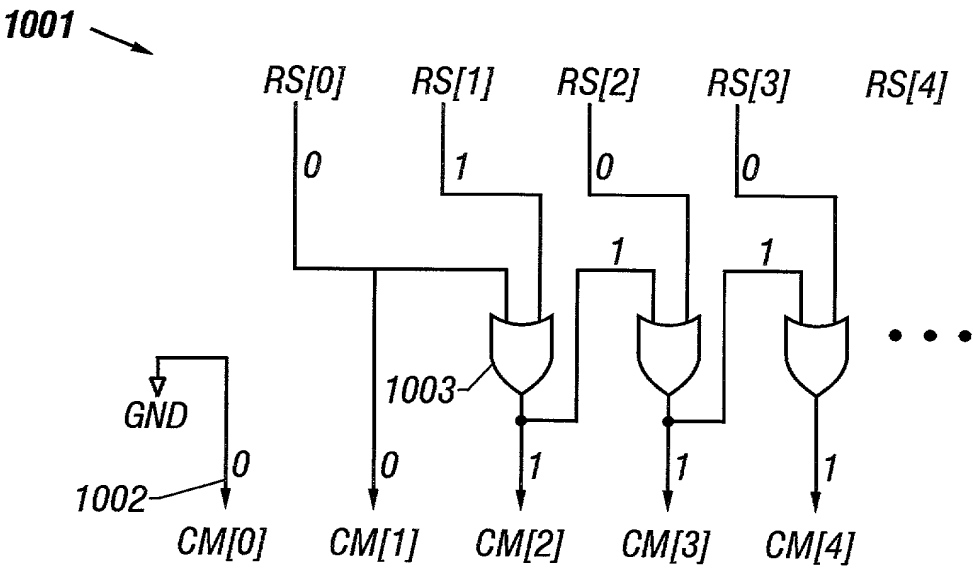


FIG. 10

1100

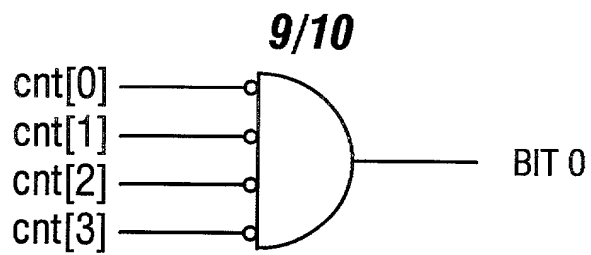
FIG. 10

900

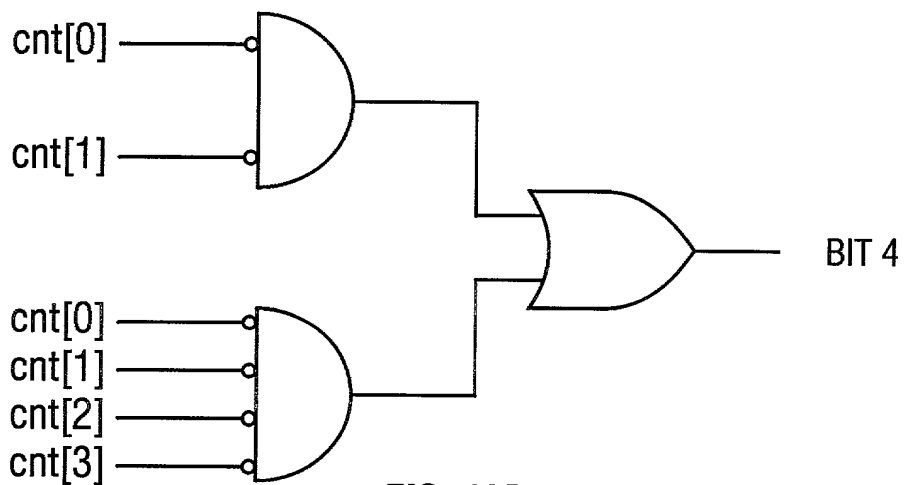
ORIGINAL MATCH BITS	0001	0100		
COUNTER VALUE = 3				
DUPLICATE MATCH BITS	0001	0100	0001	0100
COUNTER MASK	0000	1111	1111	0000
MASKED MATCH BITS	0000	0100	0001	0000
CLEAR MASK	0000	0011	1111	xxxx
APPLIED MASK	0000	0100	0000	0000
ANSWER	0000	0100		

FIG. 11

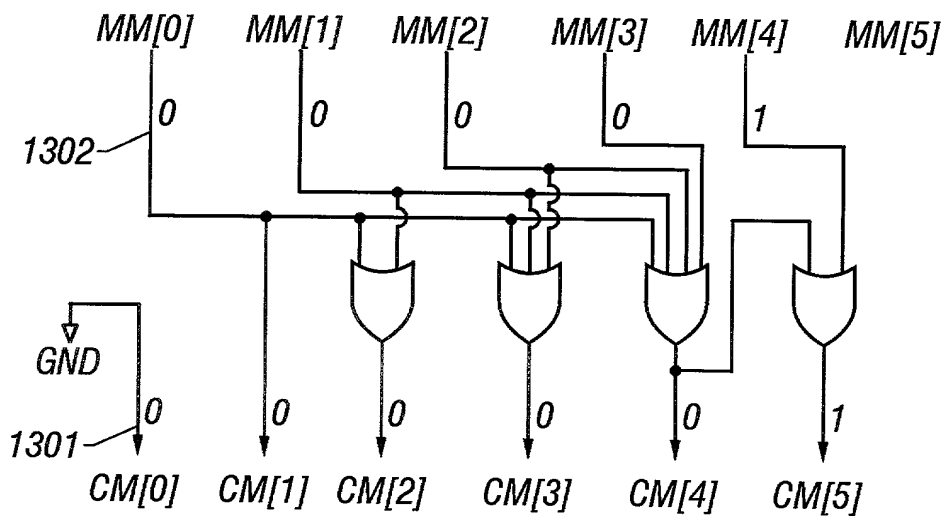




**FIG. 12A**



**FIG. 12B**



**FIG. 13**

10/10

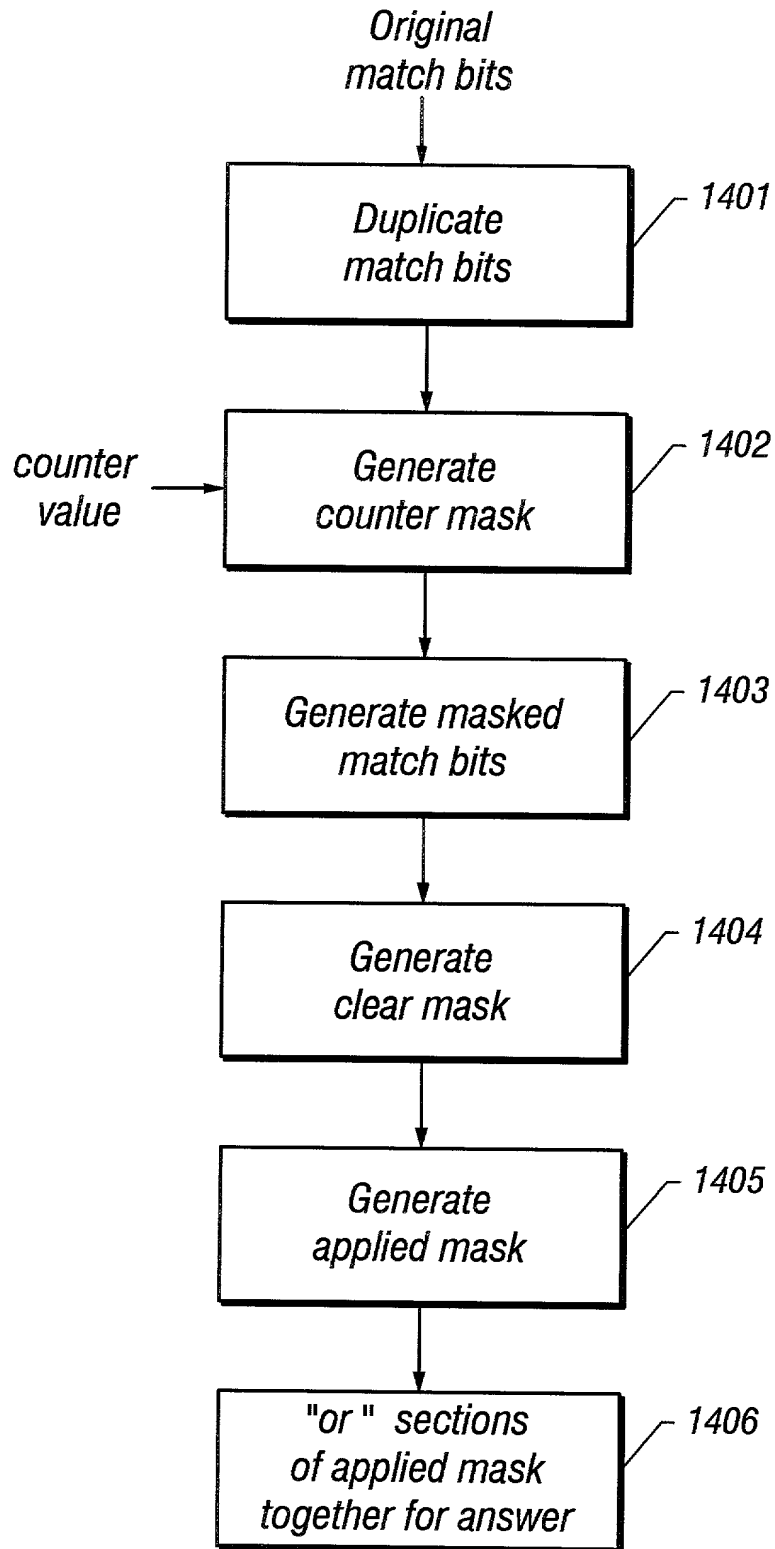


FIG. 14